CIRCUIT DEVICE FOR REALIZING A NON-LINEAR REACTIVE ELEMENTS SCALE NETWORK

FIELD OF THE INVENTION

The present invention relates to a circuit device for realizing a non-linear reactive elements scale network.

BACKGROUND OF THE INVENTION

As it is well known in this technical field, for applications relating to non-linear decoding channels for digital transmission, electronic devices capable of implementing a scale network comprising LC non-linear elements would be needed. In fact, research carried out by the Applicant indicates that a non-linear channel would provide improved performance with respect to a standard transmission channel.

For example, the here-attached Figure 1 schematically illustrates the structure of a scale network comprising *n* LC non-linear elements cascade connected together.

The network of Figure 1 is essentially a quadrupole having a pair of input terminals to which a voltage potential Vo is applied, and having a pair of output terminals to which a resistive load Rt is connected.

All the pairs of LC non-linear elements, which is L1, C1;..., Li, Ci,...,Ln, Cn, have the same value. In other words, all the L components are identical with one another, as are the C components.

In particular, the non-linear equations that the network of Figure 1 would be expected to implement are the following:

Equation (1)

$$C = \frac{C_0}{1 + \left(\frac{V_C}{V_0}\right)^2} \qquad (1)$$

where, C_0 and V_0 are constants; and

Equation (2)

$$L = \frac{L_0}{1+\left(\frac{I_L}{I_0}\right)^2} \tag{2}$$

where, L_0 and I_0 are constants.

Figure 2 shows schematically a possible circuit embodiment based on the use of a derivator.

A bipolar transistor differential cell BJT receives a bias current I1 on a first circuit branch, and it is connected to ground by a current generator I. A potential equal to Vc lies across the emitter terminals of the transistor pair.

A transistor output stage, being supplied by a current Ic, is connected to said first circuit branch and has an output terminal connected to ground through the parallel of a capacitance and a current generator.

This embodiment is based on the following approximate equation:

Equation (3)

$$\left[1+\left(\frac{V_C}{V_0}\right)^2\right]^{-1} \cong hyp\sec h^2\left(\frac{V_C}{V_0}\right) \tag{3}$$

The exponential voltage-current characteristic of the transistor pair BJT of the differential cell allows the desired non-linear equations to be synthesized where the substitution indicated in Equation (3) is carried into effect.

However, the dynamic performance of this hypothetical embodiment based on the use of a derivator would be inadequate to meet the requirements of the above application field.

If taking into consideration the non-linear capacitance alone, a possible embodiment of the network of Figure 1 could be provided through the use

of an integrator instead of a derivator. In this way, the superior dynamic characteristics of the integrator with respect to the derivator could be exploited.

An embodiment based on an integrator should implement the following operations:

Equation (4)

$$I_C = \frac{C_0}{1+\left(\frac{V_C}{V_0}\right)^2}\frac{\partial V_C}{\partial t} \Rightarrow \frac{1}{C_0}\int I_C\left[1+\left(\frac{V_C}{V_0}\right)^2\right]dt = V_C \qquad (4)$$

from which it is evinced that two multipliers would be needed.

A circuit device realized according to Equation (3) would be highly complicated. Moreover this would be even worse since the scale network of Figure 1 contains *n* LC pairs and, when the number *n* is greater than 10, as required in most applications, the complexity of the circuit embodiment would limit high-frequency performance.

SUMMARY OF THE INVENTION

The underlying technical approach to this invention is to provide a circuit device for realizing a non-linear reactive elements network, which device has suitable structural and functional features for the network to be implemented by minimizing complexity occupied area, and this without employing integrated inductors.

The principles of the present invention are based on implementing the scale network by using transconductance integrators that simulate non-linear inductors.

On the basis of the above idea, the technical problem is solved by a device as previously indicated and as defined in the characterizing part of Claim 1 herewith enclosed.

More particularly, in one embodiment the invention relates to a circuit device for realizing non-linear reactive elements scale network, wherein the non-linear elements in the network are pairs of inductive and capacitive components cascade connected between a pair of input terminals and a pair of output terminals.

The invention applies specifically to read-channel devices for hard disk drivers (HDDs), and broadly to digital communication systems, being part of a substitutive architecture of the so-called "partial-maximum likelihood response" (PRML) systems. This because it is considered that a "non-linear channel", based on the scale network as above, can provide stronger information decoding as for noise if compared to a standard scale (*e.g.*, PRML, Peak Detection, etc.).

The features and advantages of the device according to the invention will become apparent from the following description of an embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows schematically a scale network comprising *n* LC non-linear elements.

Figure 2 shows schematically a conventional circuit based on a derivator for implementing the scale network of Figure 1.

Figure 3 shows schematically a circuit device according to this invention.

Figure 4 is schematical view of the circuit detail of the device in Figure 3.

Figure 5 shows schematically a portion of the scale network according to this invention realized by means of several devices of Figure 3.

DETAILED DESCRIPTION

With reference to the drawings, in particular to the embodiments illustrated by Figures 3, 4, and 5 schematically shown is a circuit according to the invention for implementing a network 5 of reactive LC non-linear elements, *e.g.*, a network as shown schematically in Figure 1.

The device 1 has a pair of input terminals A, B on which differential input voltages Vin+ and Vin-, are respectively applied.

The device 1 also has a pair of output terminals O1, O2 where differential output voltages Vout+ and Vout- are respectively produced.

The input terminals A, B are parts of a first transconductance (Gm1) integrator 2.

The differential output pair U1, U2 of this first integrator Gm1 are connected each to a respective differential input A2, B2 of a second transconductance (Gm2) integrator 3. These outputs O1 and O2 are coupled to a feedback CMFB (Common Mode FeedBack) block 4 arranged to provide a reference signal CMFB_ref for the bias circuit portion of the second integrator 3.

In a preferred embodiment, the transconductance Gm1 of the first integrator 2 has the same value as the transconductance Gm2 of the second integrator 3. The outputs U1, U2 are also coupled to ground through respective diodes Q5 and Q6, having their high impedance input coupled to the output lines. The second integrator 3 has differential outputs that are coincident with the outputs O1 and O2 of the device 1.

The outputs O1, O2 of the device 1 are further coupled to ground through respective stabilization capacitors C_0, C_1.

Briefly, the differential input voltage Vin+, Vin- corresponds to current Ic of Equation (4), and the differential output voltage Vout+, Vout- corresponds to voltage Vc of the same Equation (4).

The integrator pair 2 and 3 basically simulate the frequency performance of a capacitance C in the scale network of Figure 1.

Also the non-linear inductor L may be implemented through an identical integrator pair design.

When implementing the inductor, L, the differential input voltage Vin+, Vin- corresponds to voltage V of the inductor, and the differential output voltage Vout+, Vout- corresponds to current I_L.

The device 1 of this invention has, therefore, no integrated inductors, so that the circuit complexity and overall occupied area of the device can be minimized.

Figure 4 schematically shows in greater circuit detail the structure of device 1.

In one embodiment, both the first and the second integrators 2 and 3, respectively are formed with mixed bipolar-MOS technology by means of bipolar transistor differential cells biased by MOS circuit portions. Other circuit designs may be used.

The first integrator 2 comprises a differential cell having a double pair of transistors, Q1, Q2 and Q3, Q4, which is associated with the differential inputs A, and B.

A bias circuit portion, comprising MOS transistors M1,..., M6, is arranged to couple the differential cell with the supply voltage references Vdd and the bias voltage and current references I1 and V1.

The transistors Q5, Q6 and Q7, diode configured, couple the outputs U1, U2 of the first integrator 2 to ground.

The outputs U1, U2 of the integrator 2 are connected to the respective inputs A2, B2 of the second integrator 3, the latter showing a differential cell structure of bipolar transistors with a double pair of input transistors Q8, Q9 and Q10, Q11.

A bias circuit portion comprised of MOS transistors M7, M8, M9 and M10 couples the differential cell of integrator 3.

A feedback block 4 connects the outputs O1, O2 of the second integrator 3 to the bias circuit portion in order to provide a voltage reference CMFB_ref for the transistor pair M7, M9.

A capacitance with value Co/2 is inserted across the outputs O1 and O2.

As said before, the device 1 allows the performance of one of the non-linear components of the scale network of Figure 1, both the capacitive component C and the inductive component L, to be emulated.

Thus, the scale network structure can be reconstructed by using a plurality of suitably interconnected devices 1.

Shown in Figure 5 is an exemplary portion of a scale network realized by connecting several devices 1 together, which are similar to the device described hereinabove.

Figure 5 shows a first device 1, emulating a first inductor L1, as being connected to the voltage generator Vo at the first differential input A.

The output O1 is connected to ground, and the output O2 is connected to the differential input A of a second device 1 emulating the capacitor C1.

The output O2 of the second device emulating C1, is connected to the differential input B of the first device emulating L1.

The output O1 of the second emulating C1, is connected to the differential input A of a third device 1 emulating a second inductor L2 in the scale network.

The output O1 of the third device emulating L2 is connected to the differential input B of the second device emulating C1, and so on.

In this way, a non-linear scale network can be implemented with at least twenty LC elements, without using integrated inductors.

The network implemented with a cascade of devices 1 according to the invention has shown to have excellent characteristics of frequency response.

In addition, the total circuit area occupied by the cascade of devices 1 is smaller than that required by conventional designs.

Lastly, the non-linear scale network of the invention allows a cascade connection of many more elements than in conventional designs.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.